

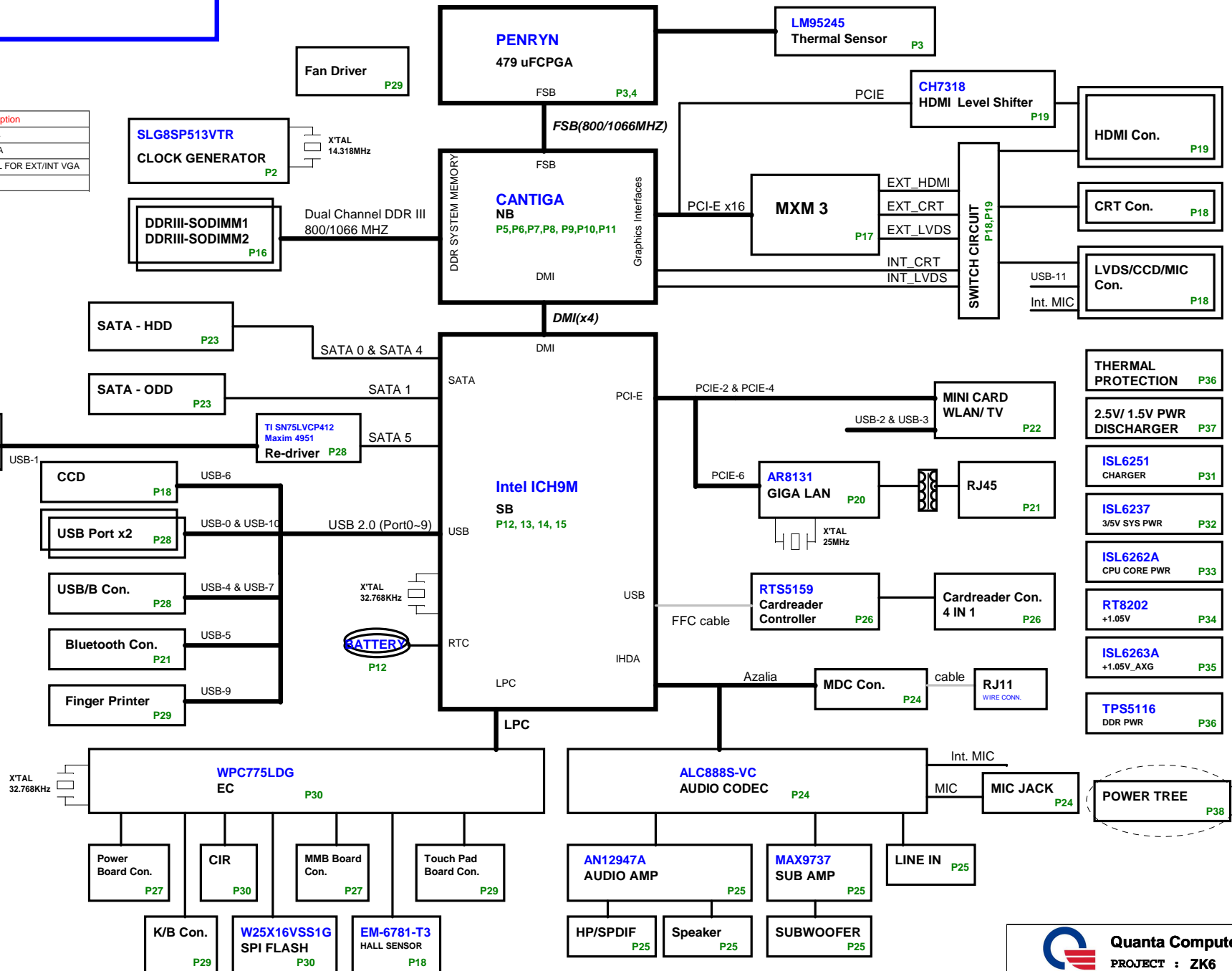
VER : 1A

ZK6 MB Block Diagram

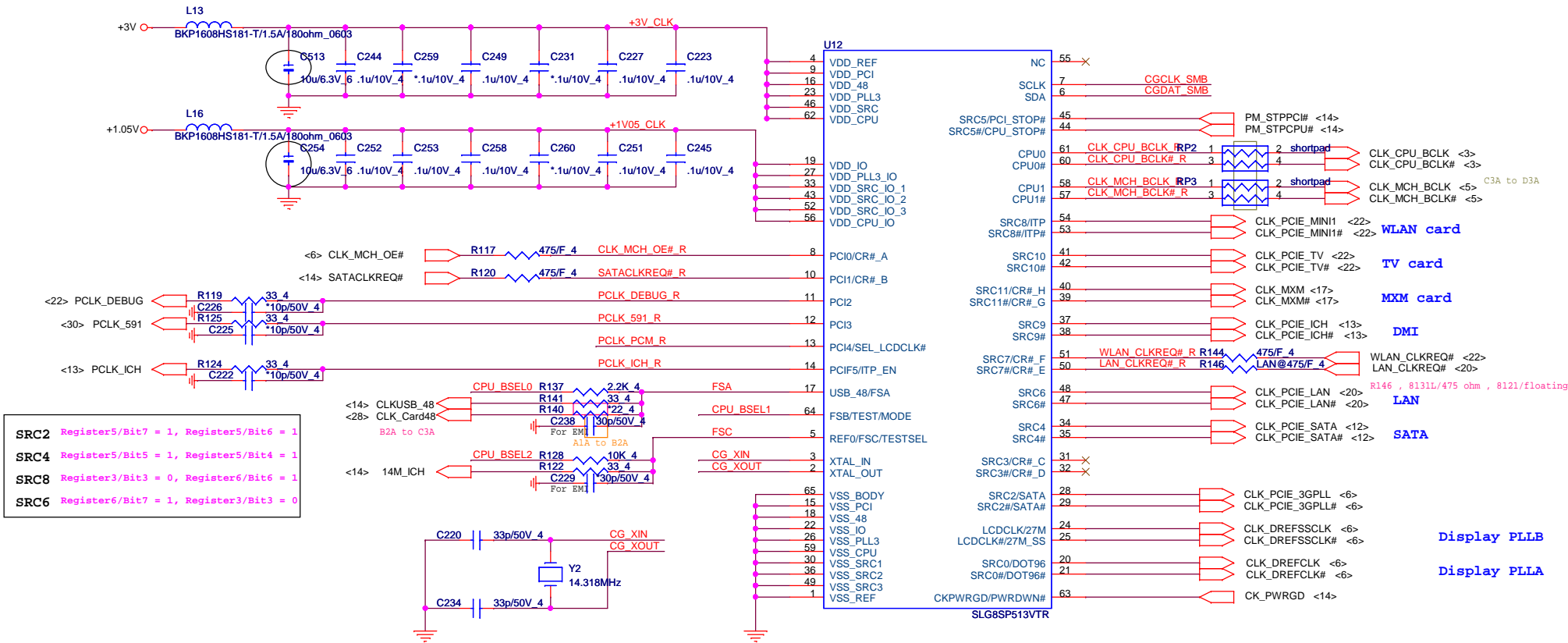
BOM P/N	Description
312K6NB0000	
412K6CS0000	
512K6S00000	USBA / BIOS
312K6NB0010	00 / 10
412K6CS0010	
512K6S00010	

BOM Option Table

Reference	Description
I@	INT VGA
E@	EXT VGA
SP@	SPECIAL FOR EXT/INT VGA
*	DNI



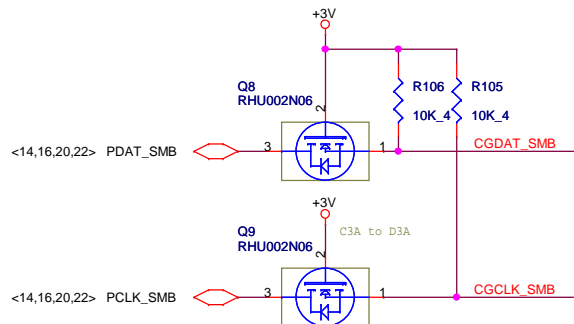
Clock Generator



CPU Clock select




FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

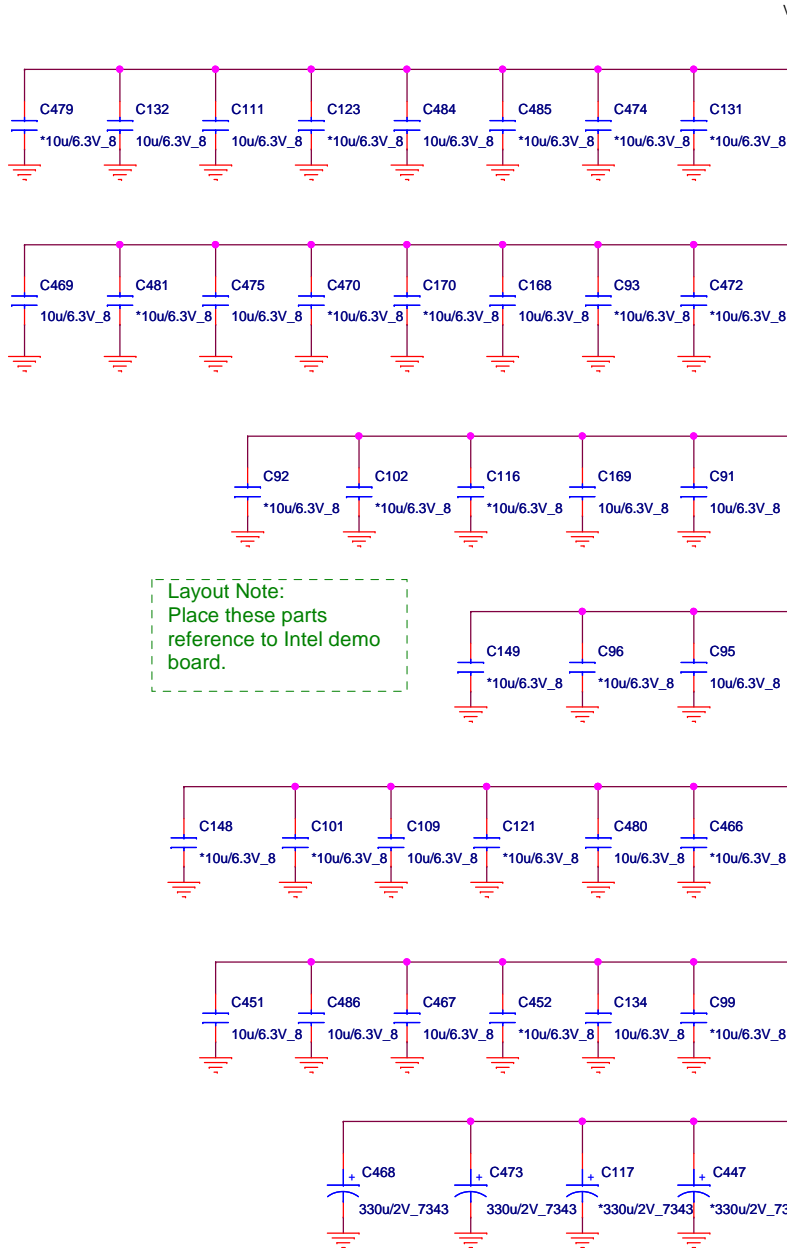
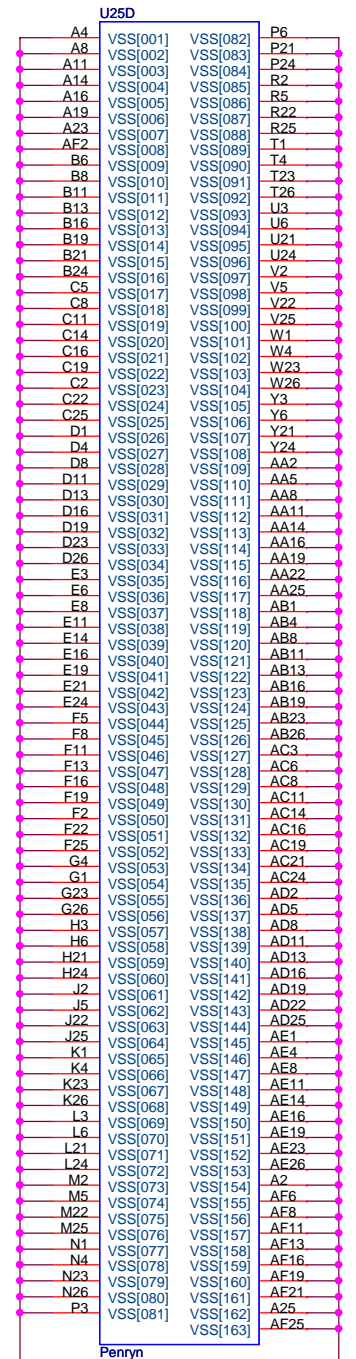


Clock Generator Strap table

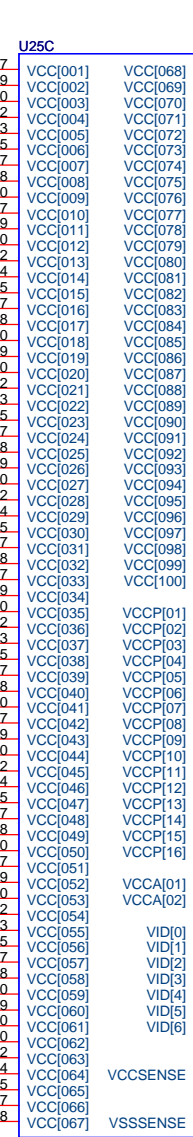


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PROJECT : ZK6

Size	Document Number	Rev 1A
CLOCK GENERATOR		
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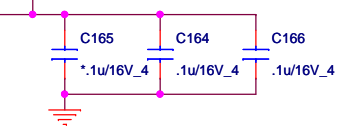
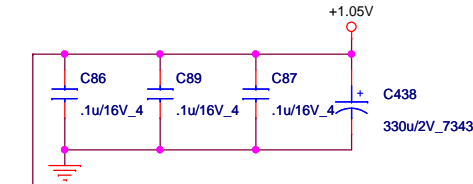
Layout Note:
Place these parts
reference to Intel demo
board.



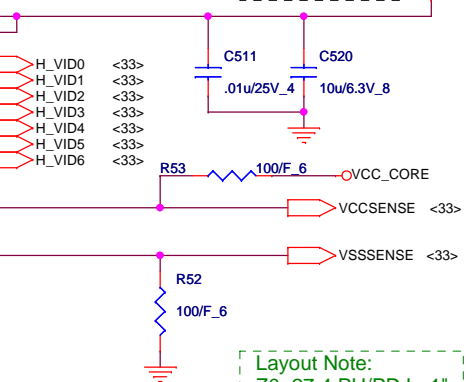
VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA:130mA



Layout Note:
Z0=27.4,PJ/PD L<1"

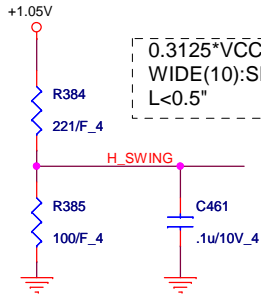
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2



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CPU Power		
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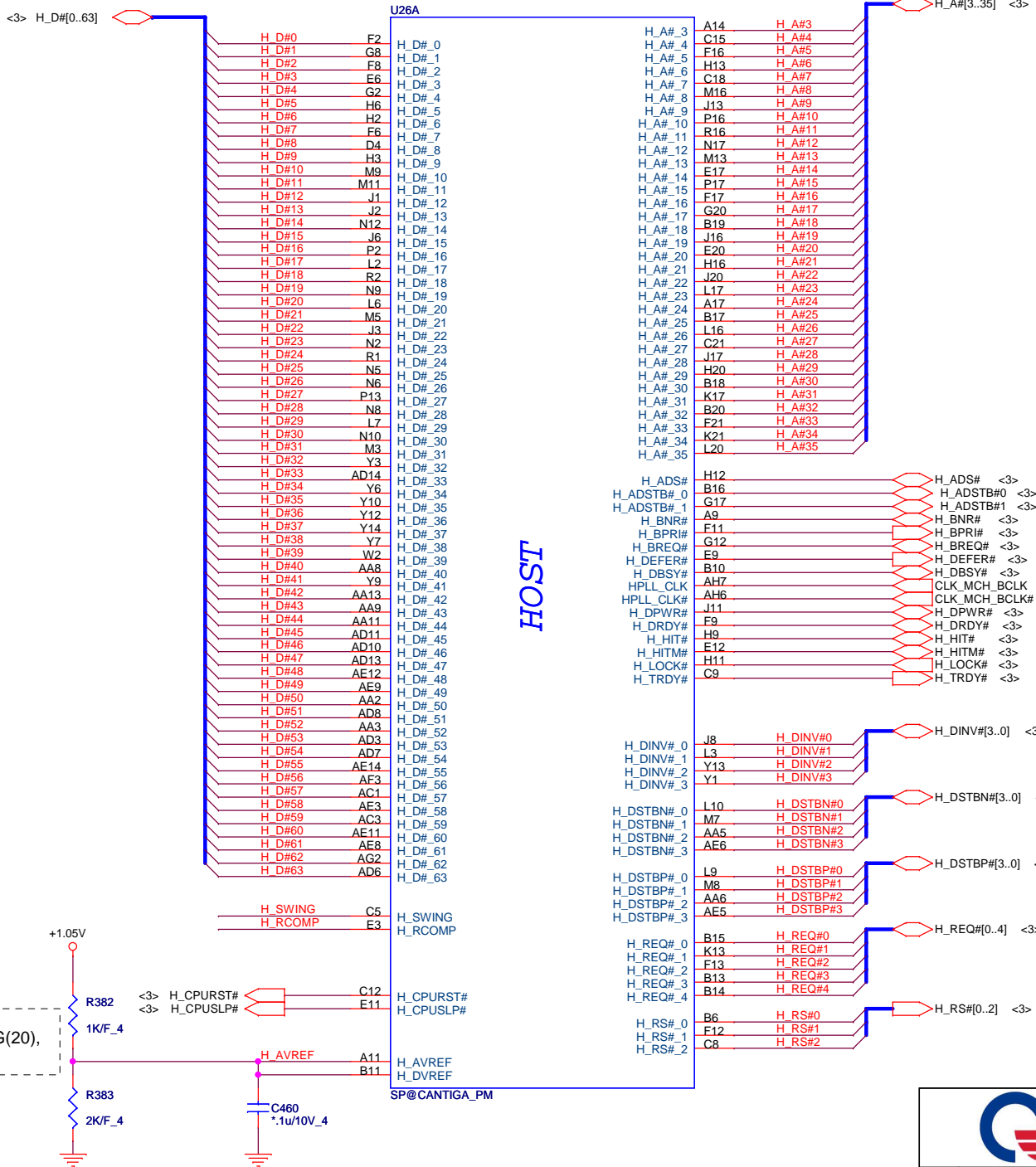
	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06




0.3125*VCCP
WIDE(10):SPACING(20),
L<0.5"

Layout Note:
WIDE(10):SPACING(20),
L<0.5"

2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"



GMCH (CANTIGA)



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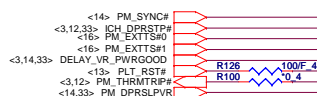
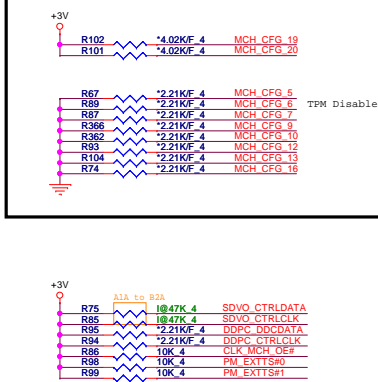
GMCH HOST

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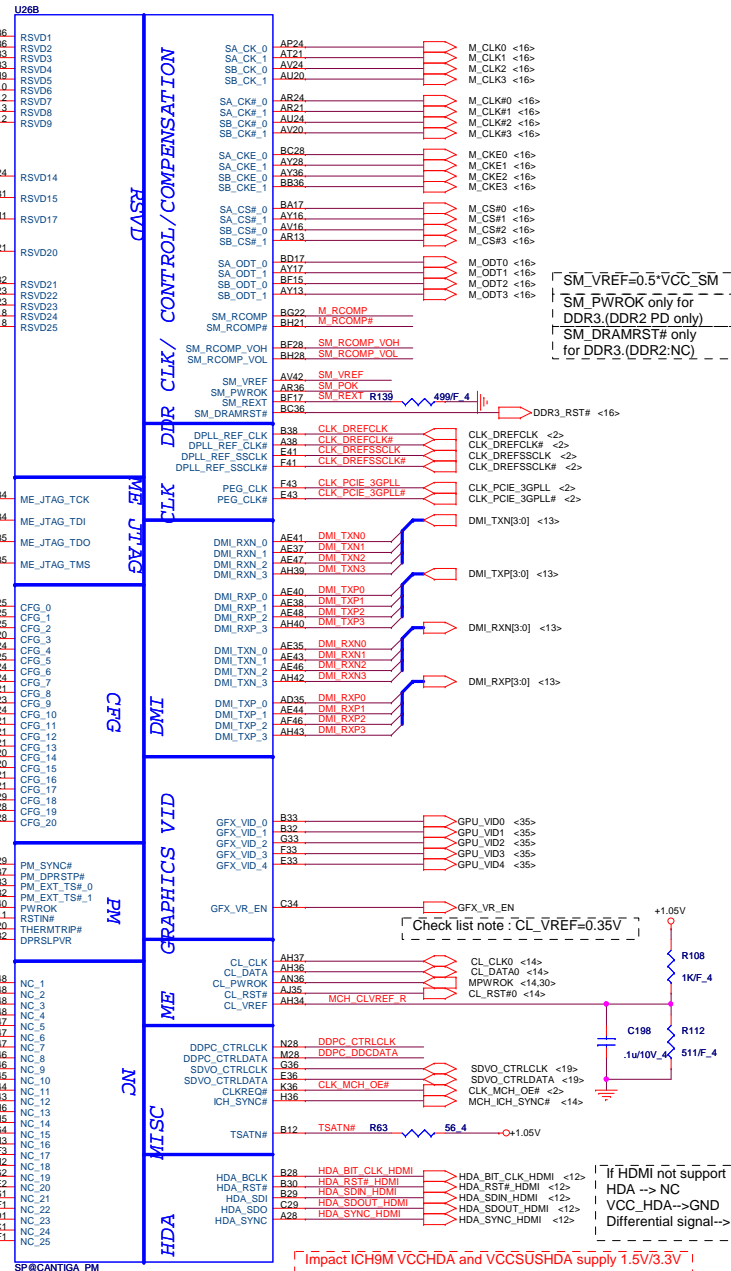
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	ITPM Host Interface	0 = ITPM Host Interface is enabled 1 = ITPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent (Default) 1 = Digital display(HDMI/DP) device present

Strap pin



NB Thermal trip pin
No use Thermal trip NB side can NC (NB has ODT)
PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (GMCH and CPU, in that order).



If LVDS no use, all signal can NC



DDR SYSTEM MEMORY A

M_A_DQ0	AJ38	SA_DQ_0
M_A_DQ1	AJ41	SA_DQ_1
M_A_DQ2	AN38	SA_DQ_2
M_A_DQ3	AM38	SA_DQ_3
M_A_DQ4	AJ36	SA_DQ_4
M_A_DQ5	AJ40	SA_DQ_5
M_A_DQ6	AM44	SA_DQ_6
M_A_DQ7	AM42	SA_DQ_7
M_A_DQ8	AN43	SA_DQ_8
M_A_DQ9	AN44	SA_DQ_9
M_A_DQ10	AU40	SA_DQ_10
M_A_DQ11	AT38	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AU44	SA_DQ_14
M_A_DQ15	AU42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AY41	SA_DQ_20
M_A_DQ21	AY43	SA_DQ_21
M_A_DQ22	BB41	SA_DQ_22
M_A_DQ23	BC40	SA_DQ_23
M_A_DQ24	AY37	SA_DQ_24
M_A_DQ25	BD38	SA_DQ_25
M_A_DQ26	AY37	SA_DQ_26
M_A_DQ27	AT36	SA_DQ_27
M_A_DQ28	AY38	SA_DQ_28
M_A_DQ29	BB38	SA_DQ_29
M_A_DQ30	AV36	SA_DQ_30
M_A_DQ31	AW36	SA_DQ_31
M_A_DQ32	BD13	SA_DQ_32
M_A_DQ33	AU11	SA_DQ_33
M_A_DQ34	BC11	SA_DQ_34
M_A_DQ35	BA12	SA_DQ_35
M_A_DQ36	AU13	SA_DQ_36
M_A_DQ37	AV13	SA_DQ_37
M_A_DQ38	BD12	SA_DQ_38
M_A_DQ39	BC12	SA_DQ_39
M_A_DQ40	BB9	SA_DQ_40
M_A_DQ41	BA9	SA_DQ_41
M_A_DQ42	AU10	SA_DQ_42
M_A_DQ43	AV9	SA_DQ_43
M_A_DQ44	BA11	SA_DQ_44
M_A_DQ45	BD9	SA_DQ_45
M_A_DQ46	AY8	SA_DQ_46
M_A_DQ47	BA6	SA_DQ_47
M_A_DQ48	AV5	SA_DQ_48
M_A_DQ49	AV7	SA_DQ_49
M_A_DQ50	AT9	SA_DQ_50
M_A_DQ51	AN8	SA_DQ_51
M_A_DQ52	AU5	SA_DQ_52
M_A_DQ53	AU6	SA_DQ_53
M_A_DQ54	AT5	SA_DQ_54
M_A_DQ55	AN10	SA_DQ_55
M_A_DQ56	AM11	SA_DQ_56
M_A_DQ57	AM5	SA_DQ_57
M_A_DQ58	AJ9	SA_DQ_58
M_A_DQ59	AJ8	SA_DQ_59
M_A_DQ60	AN12	SA_DQ_60
M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

SP@CANTIGA_PM

SA_BS_0	BD21	M_A_BS0 <16>
SA_BS_1	BG18	M_A_BS1 <16>
SA_BS_2	AT25	M_A_BS2 <16>
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SA_CAS#	BD20	M_A_CAS# <16>
SA_WE#	AY20	M_A_WE# <16>
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SA_DM_1	AT41	M_A_DM1
SA_DM_2	AY41	M_A_DM2
SA_DM_3	AU39	M_A_DM3
SA_DM_4	BB12	M_A_DM4
SA_DM_5	AY6	M_A_DM5
SA_DM_6	AT7	M_A_DM6
SA_DM_7	AJ5	M_A_DM7
SA_DQS_0	AJ44	M_A_DQS0
SA_DQS_1	AT44	M_A_DQS1
SA_DQS_2	BA43	M_A_DQS2
SA_DQS_3	BC37	M_A_DQS3
SA_DQS_4	AW12	M_A_DQS4
SA_DQS_5	BC8	M_A_DQS5
SA_DQS_6	AU8	M_A_DQS6
SA_DQS_7	AM7	M_A_DQS7
SA_DQS#_0	AJ43	M_A_DQS#0
SA_DQS#_1	AT43	M_A_DQS#1
SA_DQS#_2	BA44	M_A_DQS#2
SA_DQS#_3	BD37	M_A_DQS#3
SA_DQS#_4	AY12	M_A_DQS#4
SA_DQS#_5	BD8	M_A_DQS#5
SA_DQS#_6	AU9	M_A_DQS#6
SA_DQS#_7	AM8	M_A_DQS#7
SA_MA_0	BA21	M_A_A0
SA_MA_1	BC24	M_A_A1
SA_MA_2	BG24	M_A_A2
SA_MA_3	BH24	M_A_A3
SA_MA_4	BG25	M_A_A4
SA_MA_5	BA24	M_A_A5
SA_MA_6	BD24	M_A_A6
SA_MA_7	BG27	M_A_A7
SA_MA_8	BF25	M_A_A8
SA_MA_9	AW24	M_A_A9
SA_MA_10	BC21	M_A_A10
SA_MA_11	BG26	M_A_A11
SA_MA_12	BH26	M_A_A12
SA_MA_13	BH17	M_A_A13
SA_MA_14	AY25	M_A_A14

M_A_DM[7:0] <16>	M_A_DM0	M_A_DM1	M_A_DM2	M_A_DM3	M_A_DM4	M_A_DM5	M_A_DM6	M_A_DM7
M_A_DQS[7:0] <16>	M_A_DQS0	M_A_DQS1	M_A_DQS2	M_A_DQS3	M_A_DQS4	M_A_DQS5	M_A_DQS6	M_A_DQS7
M_A_DQS#[7:0] <16>	M_A_DQS#0	M_A_DQS#1	M_A_DQS#2	M_A_DQS#3	M_A_DQS#4	M_A_DQS#5	M_A_DQS#6	M_A_DQS#7
M_A_A[14:0] <16>	M_A_A0	M_A_A1	M_A_A2	M_A_A3	M_A_A4	M_A_A5	M_A_A6	M_A_A7

<16> M_B_DQ[63:0]

M_B_DQ0	AK47	SB_DQ_0
M_B_DQ1	AH46	SB_DQ_1
M_B_DQ2	AP47	SB_DQ_2
M_B_DQ3	AP46	SB_DQ_3
M_B_DQ4	AJ46	SB_DQ_4
M_B_DQ5	AJ48	SB_DQ_5
M_B_DQ6	AM48	SB_DQ_6
M_B_DQ7	AP48	SB_DQ_7
M_B_DQ8	AJ47	SB_DQ_8
M_B_DQ9	AJ46	SB_DQ_9
M_B_DQ10	BA48	SB_DQ_10
M_B_DQ11	AY48	SB_DQ_11
M_B_DQ12	AT47	SB_DQ_12
M_B_DQ13	AR47	SB_DQ_13
M_B_DQ14	BA47	SB_DQ_14
M_B_DQ15	BC47	SB_DQ_15
M_B_DQ16	BC46	SB_DQ_16
M_B_DQ17	BC44	SB_DQ_17
M_B_DQ18	BG43	SB_DQ_18
M_B_DQ19	BF43	SB_DQ_19
M_B_DQ20	BF45	SB_DQ_20
M_B_DQ21	BC41	SB_DQ_21
M_B_DQ22	BF40	SB_DQ_22
M_B_DQ23	BF41	SB_DQ_23
M_B_DQ24	BG38	SB_DQ_24
M_B_DQ25	BF38	SB_DQ_25
M_B_DQ26	BH35	SB_DQ_26
M_B_DQ27	BG35	SB_DQ_27
M_B_DQ28	BH40	SB_DQ_28
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M_B_DQ30	BG34	SB_DQ_30
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M_B_DQ32	BH14	SB_DQ_32
M_B_DQ33	BG12	SB_DQ_33
M_B_DQ34	BH11	SB_DQ_34
M_B_DQ35	BG8	SB_DQ_35
M_B_DQ36	BH12	SB_DQ_36
M_B_DQ37	BF11	SB_DQ_37
M_B_DQ38	BF8	SB_DQ_38
M_B_DQ39	BG7	SB_DQ_39
M_B_DQ40	BC5	SB_DQ_40
M_B_DQ41	BC6	SB_DQ_41
M_B_DQ42	AY3	SB_DQ_42
M_B_DQ43	AY1	SB_DQ_43
M_B_DQ44	BF6	SB_DQ_44
M_B_DQ45	BF5	SB_DQ_45
M_B_DQ46	BA1	SB_DQ_46
M_B_DQ47	BD3	SB_DQ_47
M_B_DQ48	AV2	SB_DQ_48
M_B_DQ49	AU3	SB_DQ_49
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M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ1	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
M_B_DQ61	AM3	SB_DQ_61
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SP@CANTIGA_PM

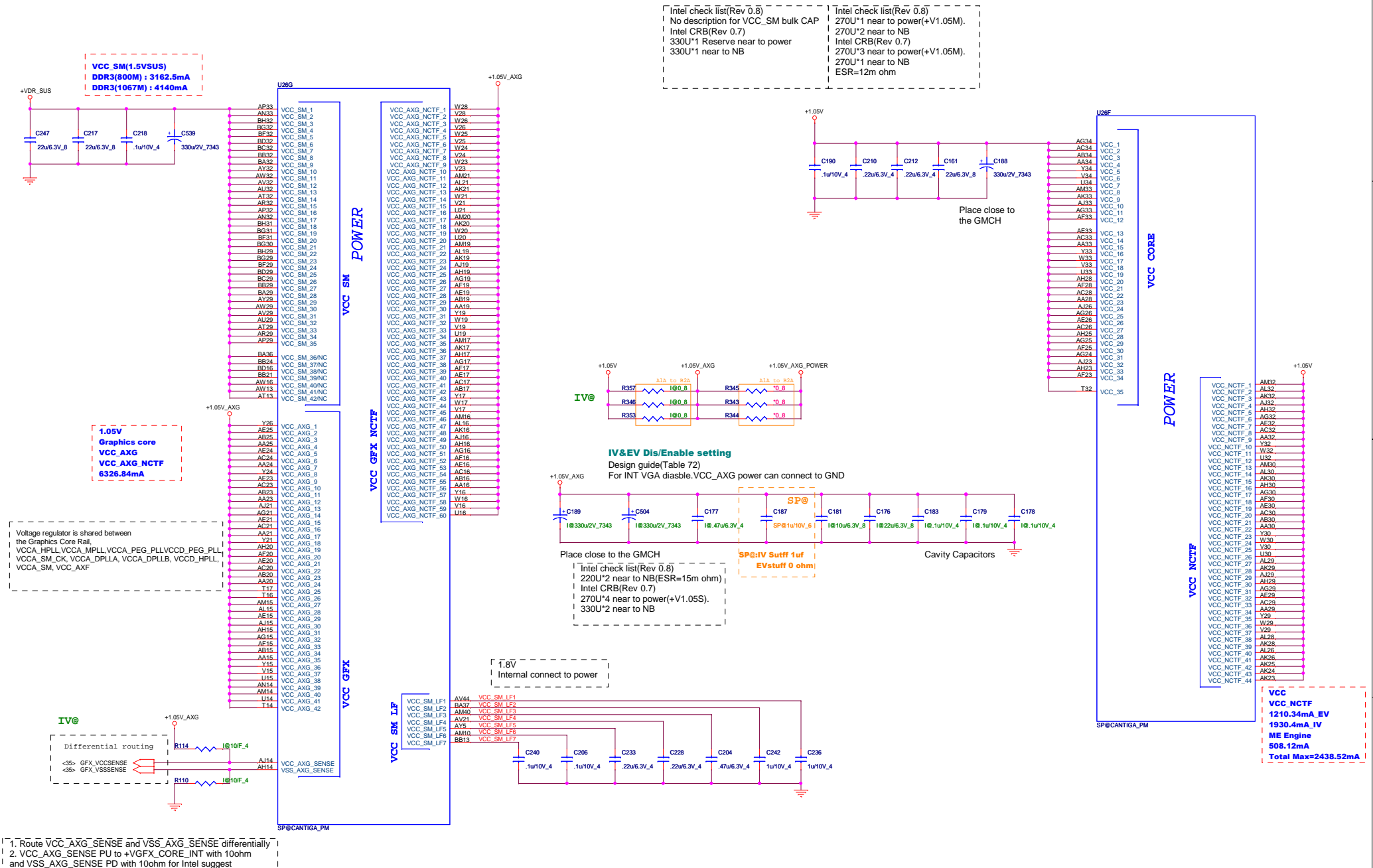
DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0 <16>
SB_BS_1	BB17	M_B_BS1 <16>
SB_BS_2	BB33	M_B_BS2 <16>
SB_RAS#	AU17	M_B_RAS# <16>
SB_CAS#	BG16	M_B_CAS# <16>
SB_WE#	BF14	M_B_WE# <16>
SB_DM_0	AM47	M_B_DM0
SB_DM_1	AY47	M_B_DM1
SB_DM_2	BD40	M_B_DM2
SB_DM_3	BF35	M_B_DM3
SB_DM_4	BG11	M_B_DM4
SB_DM_5	BA3	M_B_DM5
SB_DM_6	AP1	M_B_DM6
SB_DM_7	AK2	M_B_DM7
SB_DQS_0	AL47	M_B_DQS0
SB_DQS_1	AV48	M_B_DQS1
SB_DQS_2	BG41	M_B_DQS2
SB_DQS_3	BG37	M_B_DQS3
SB_DQS_4	BH9	M_B_DQS4
SB_DQS_5	BB2	M_B_DQS5
SB_DQS_6	AU1	M_B_DQS6
SB_DQS_7	AN6	M_B_DQS7
SB_DQS#_0	AL46	M_B_DQS#0
SB_DQS#_1	AV47	M_B_DQS#1
SB_DQS#_2	BH41	M_B_DQS#2
SB_DQS#_3	BH37	M_B_DQS#3
SB_DQS#_4	BG9	M_B_DQS#4
SB_DQS#_5	BC2	M_B_DQS#5
SB_DQS#_6	AT2	M_B_DQS#6
SB_DQS#_7	AN5	M_B_DQS#7
SB_MA_0	AV17	M_B_A0
SB_MA_1	BA25	M_B_A1
SB_MA_2	BC25	M_B_A2
SB_MA_3	AU25	M_B_A3
SB_MA_4	AW25	M_B_A4
SB_MA_5	BB28	M_B_A5
SB_MA_6	AU28	M_B_A6
SB_MA_7	AW28	M_B_A7
SB_MA_8	AT33	M_B_A8
SB_MA_9	BD33	M_B_A9
SB_MA_10	BB16	M_B_A10
SB_MA_11	AW33	M_B_A11
SB_MA_12	AY33	M_B_A12
SB_MA_13	BH15	M_B_A13
SB_MA_14	AU33	M_B_A14



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GMCH DDRIII		
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IV@
EV@
SP@

1210 100uH, 10%,
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL A/B

1210 100uH, 10%,
0.45A DCR_max = 0.39

VCCA_DPLL/A/B always keep to +1.05V
(If no use IV dynamic core power)

1210 0.1uH, 20%, 1A,
DCR_max=0.078Q

3.3V
24.15mA for VCCA_TV_DAC
39.48mA for VCCA_TV_B_DAC
24.15mA for VCCA_TV_C_DAC
Total 87.78mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
48.363mA for CRT
5mA for TV

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

FB 220 @100 MHz, 25%, 2A

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting
SP@iNT use 0.1U
EXT use 0 ohm

IV&EV Dis/Enable setting
SP@iNT use 0.1U
EXT use 0 ohm

IV&EV Dis/Enable setting
SP@iNT use 1 U
EXT use 0 ohm

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

Check list : 0.1uH
CRB : 0 ohm
1210 0.1 ?H, 20% 1A
DCR max = 78 m

Clock supply(1.5V)
DDR3(1066):149.5mA

D805 1UH, Rdc = 0.14 - 0.26.
Max rated current = 220 mA

0805 100 nH, DCR=160 m

LVDS Transmitter(1.8V)
118.8mA

POWER

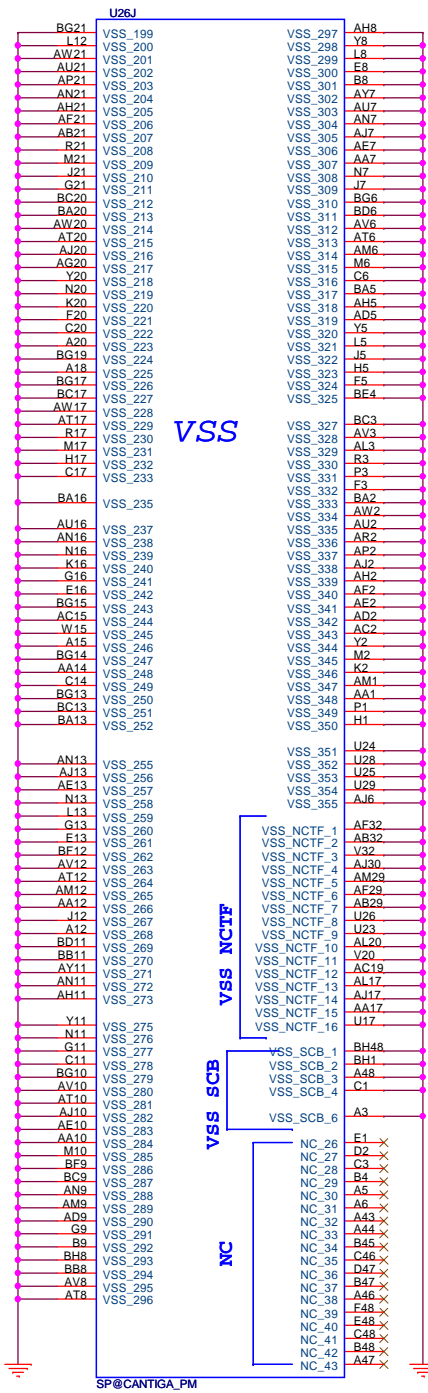
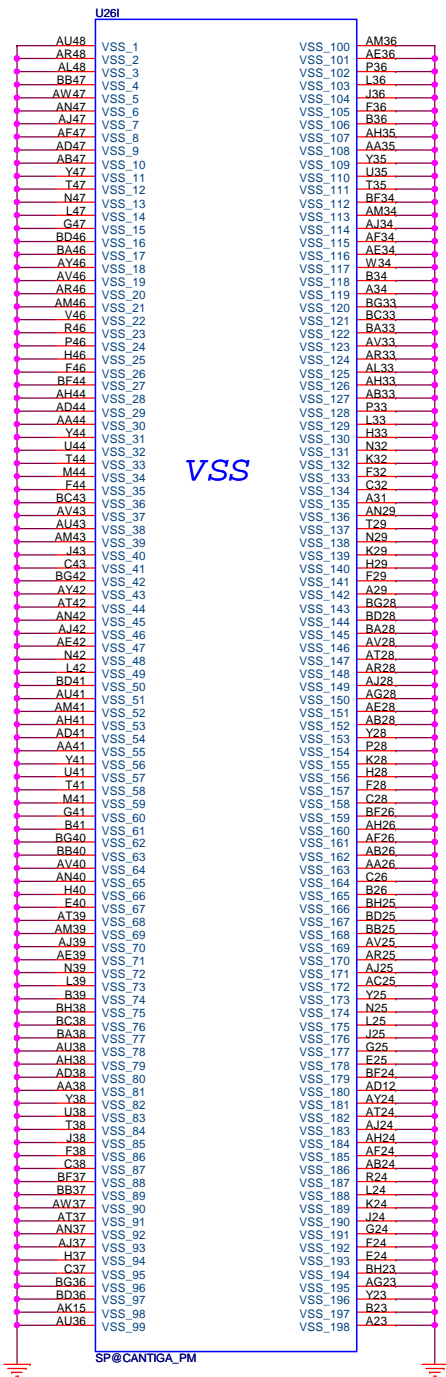
Power Net Name	Cantiga(V)
VCC_AXG_#	1.05V
VCC_AXG_NCTF_#	
VCCA_PEG_BG	1.5V
VCCA_DPLL_A	1.05V
VCCA_DPLL_B	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

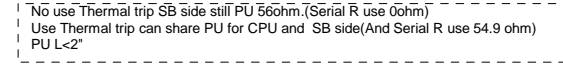


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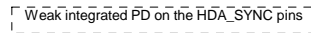
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GMCH POWER

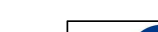






HD Audio

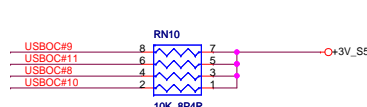
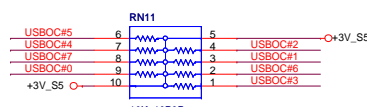
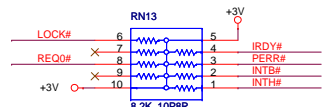
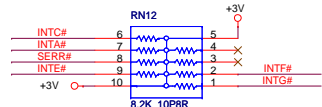
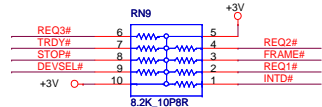
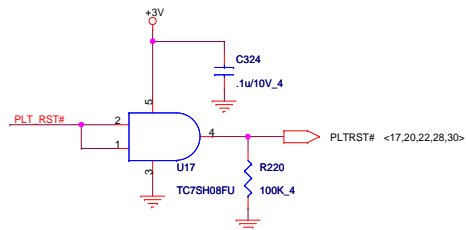
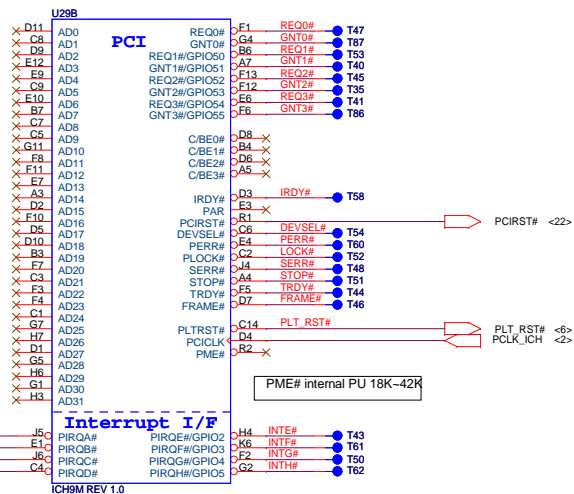


RTC



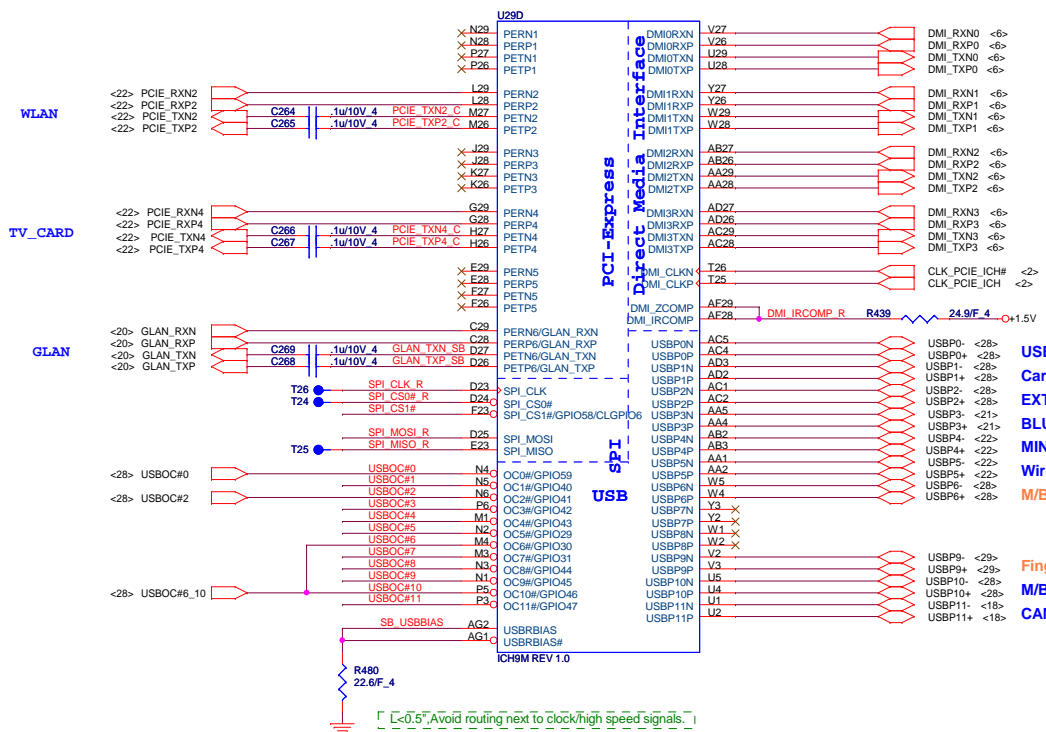
South Bridge Strap Pin (1/3)

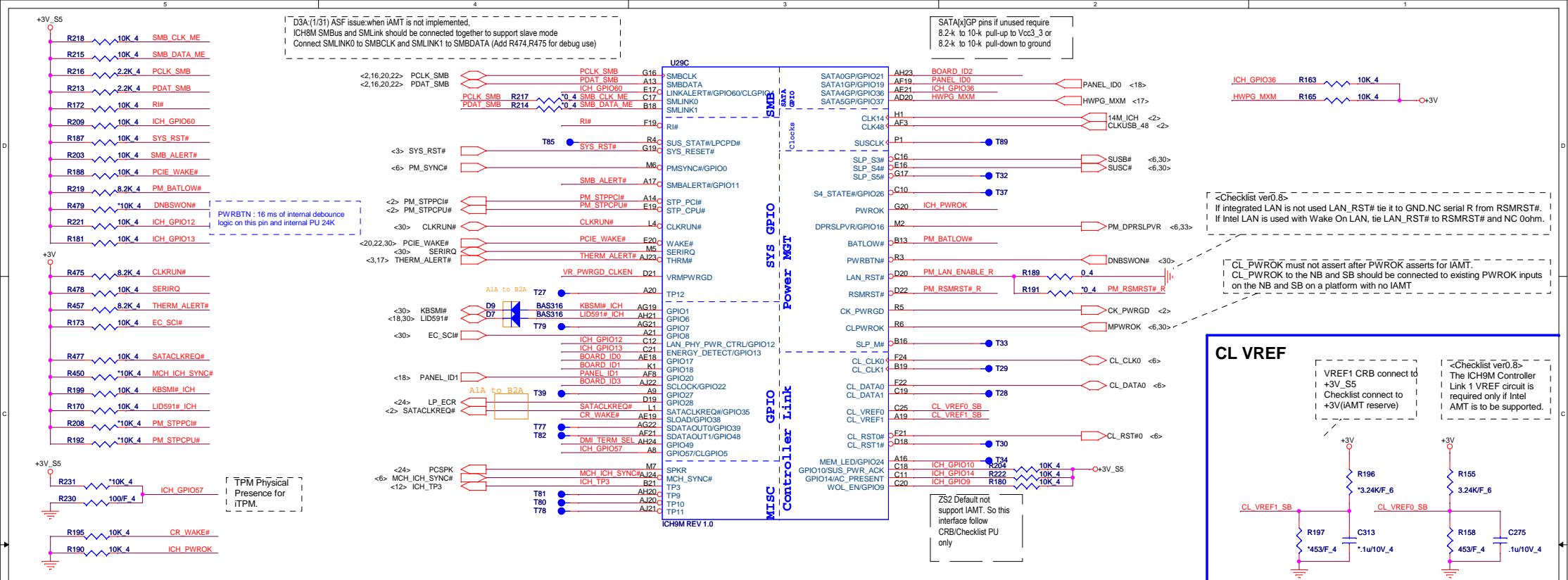
Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	<14> 
			0	0	RSVD	
			0	1	Enter XOR Chain	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	1	0	Normal operation(Default)	
			1	1	Set PCIe port config bit 1	



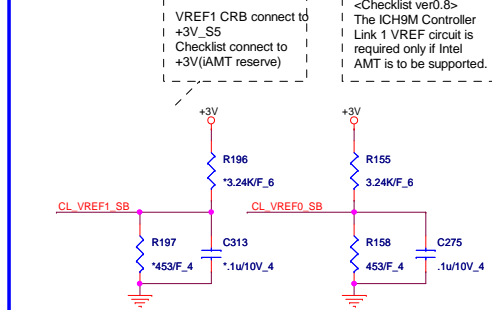
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R485 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R156 *10K_4
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 SPL_CS#1 Boot Location	GNT0# R486 *1K_4
SPL_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	0 1	SPL_CS1# R177 *1K_4
			1 1	

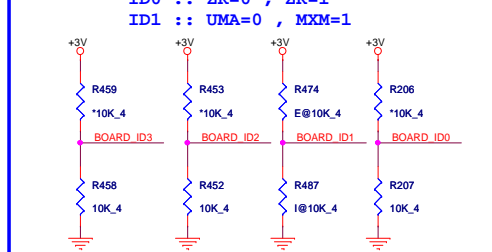




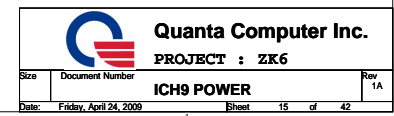
CL VREF

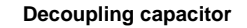


M/B ID

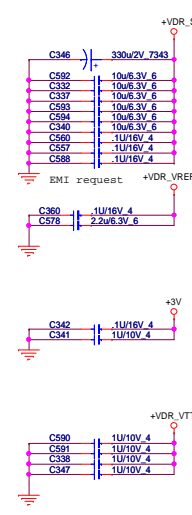


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

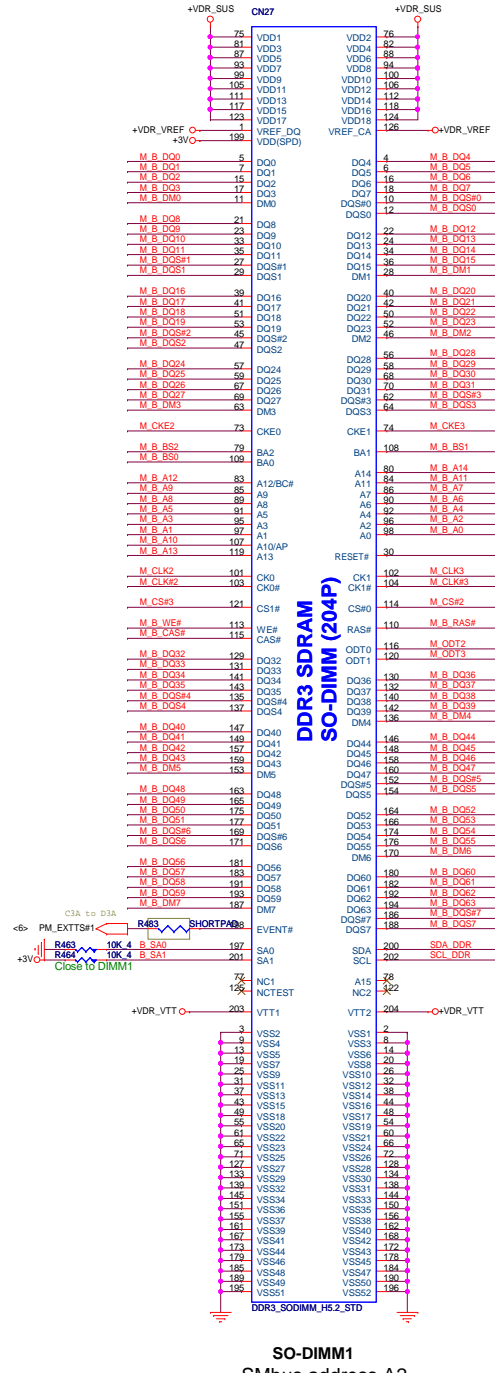




Close to SO-DIMM

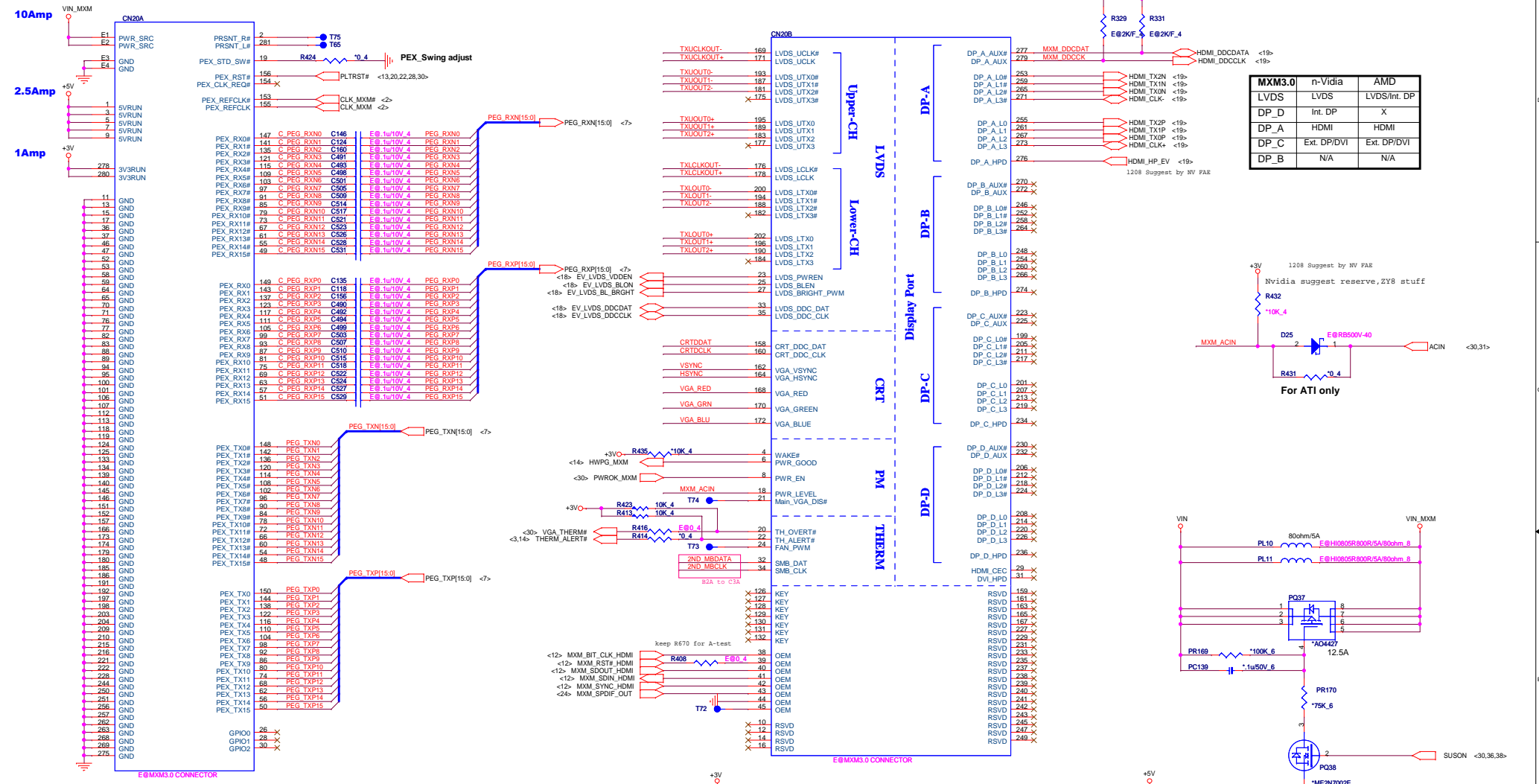


DDR3 SDRAM
SO-DIMM (2041

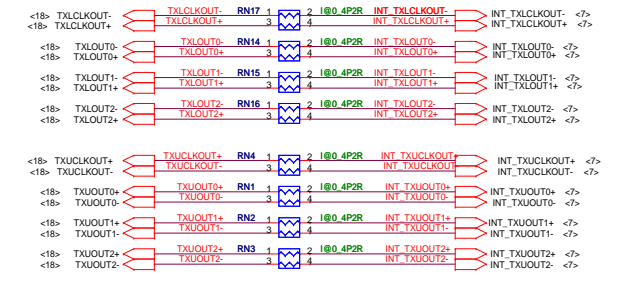


SO-DIMM1
SMBus address A2

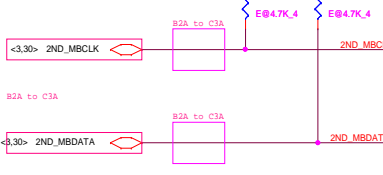
MXM Module



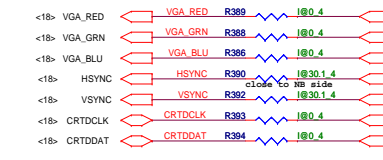
LVDS



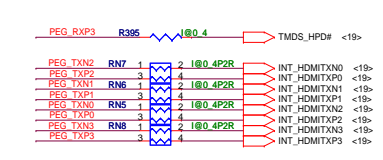
Thermo SMBus



CRT



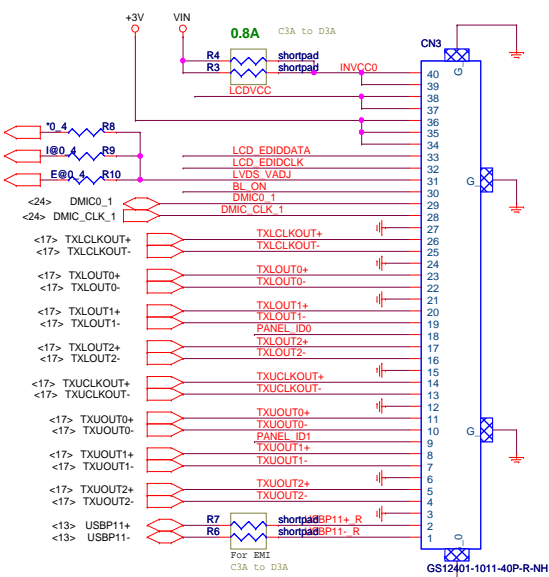
iHDMI



IV@
EV@



```
<17> EV_LVDS_BL_BRGHT
=> MXM
=> UMA
=> EC
<7> L_BKLT_CTRL
<30> CONTRAST
```



LCD Power

<7> INT_LVDS_DIGON

<17> EV_LVDS_VDDEN

R44 I@0_4

R43 F@0_4

C29 1u/10V_4

+3V

U1 AAT4280-4

IN

IN

ON/OFF

OUT

GND

GND

C13 *1u/10V_4

C17 *2.2u/10V_8

C12 .1u/10V_4

C14 .01u/25V_4

C23 22u/6.3V_8

R38 I@100K_4


LCDVCC

<Check list ver:0.8>
UMA: 100K pull-down to GND

[illegible]

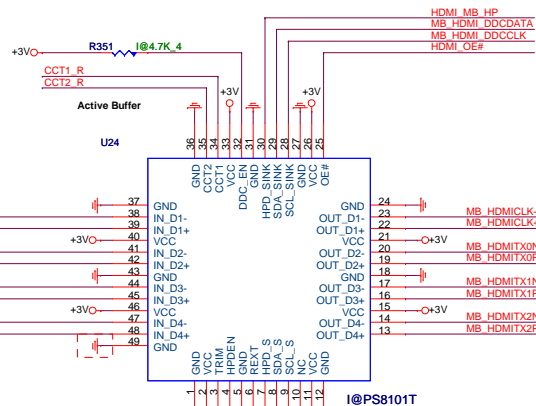
I@ HDMI LEVEL SHIFTER

To GMCH

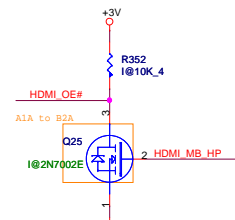
<17> TMD5_HPDP# 

Voltage level 0.9V

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB



OE# control for power saving



Switch I2C E@ or I

To MXM

<17> HDMI_DDCCLK

MB_HDMI_DDCCLK

5V0 D3 2 1 RB501V-40

+3V0

A1A to B2A

Q4 E@2N7002

R34 1.5K_4

R35 0_4

HDMI_DDCCLK_MB

SP@BLM18AG601/200mA/600ohm_6

C72 1uF/10V_4

To MXM

<17> HDMI_DDCDATA

MB_HDMI_DDCDATA

5V0 D2 2 1 RB501V-40

+3V0

A1A to B2A

Q23 E@2N7002

R33 1.5K_4

R336 0_4

HDMI_DDCDATA_MB

SP@BLM18AG601/200mA/600ohm_6

C71 1uF/10V_4

[illegible]

U7		*RClamp0524P	
1	10	10	MB_HDMITX0N
2	9	9	MB_HDMITX0P
3	9		
4	7	7	MB_HDMITX2N
5	6	6	MB_HDMITX2P
6	6		

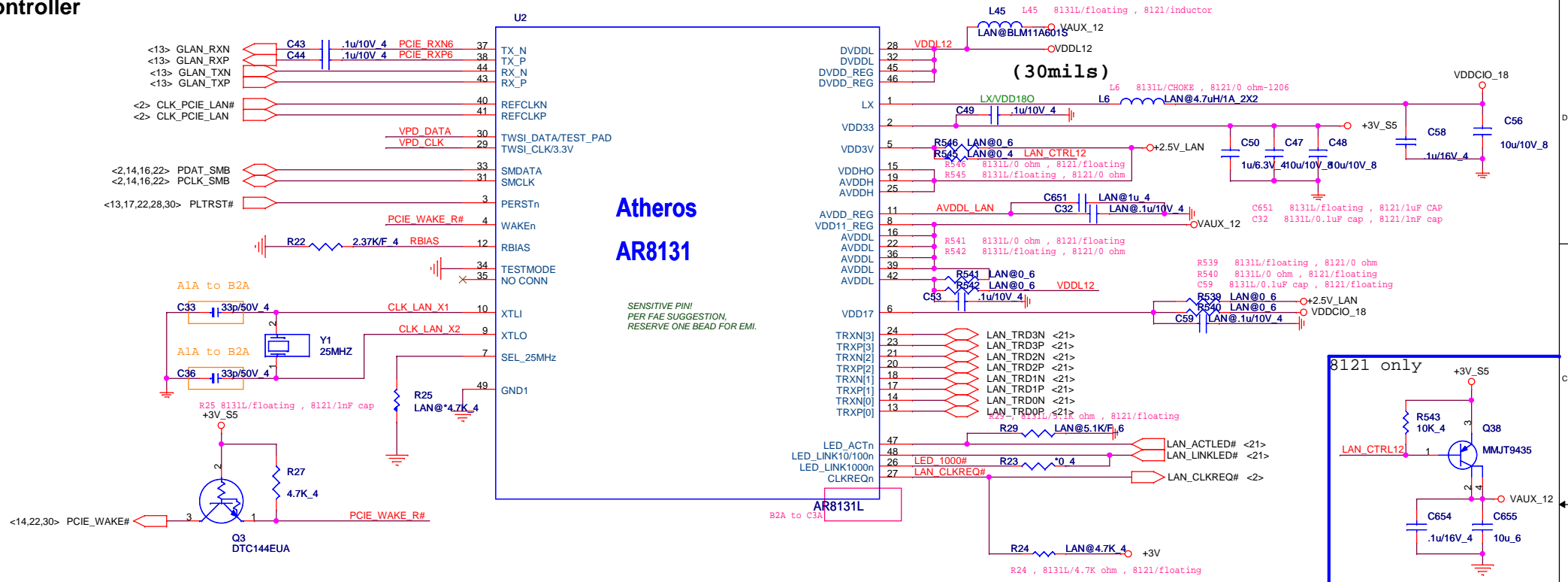
U6		*RClamp0524P	
1	10	10	MB_HDMITX1P
2	9	9	MB_HDMITX1N
3	9		
4	7	7	MB_HDMICLK+
5	6	6	MB_HDMICLK-
6	6		

U5		*RClamp0524P	
1	10	10	HDMI_DDCCLK_M
2	9	9	HDMI_DDCDATA_M
3	9		
4	7	7	HDMI_MB_HP
5	6	6	
6	6		

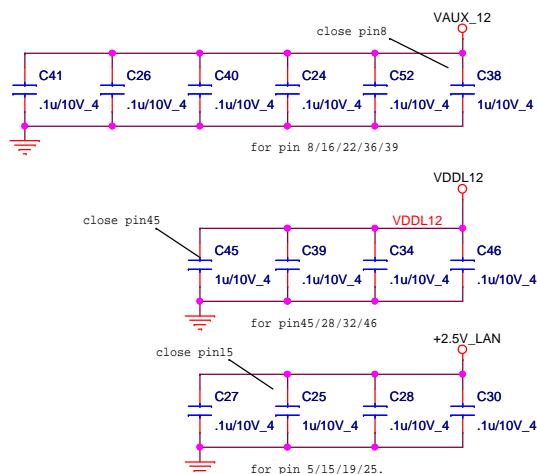
Timing diagram for A1A to B2A showing MB_HDMITX signals. The diagram shows four pairs of signals: MB_HDMITX2P and MB_HDMITX2N, MB_HDMITX1P and MB_HDMITX1N, MB_HDMITX0N and MB_HDMICLK+, and MB_HDMICLK- and MB_HDMITX0P. Each pair is associated with a resistor value of *100/F₄ and a delay of R529, R530, R531, or R532 respectively.

[illegible]

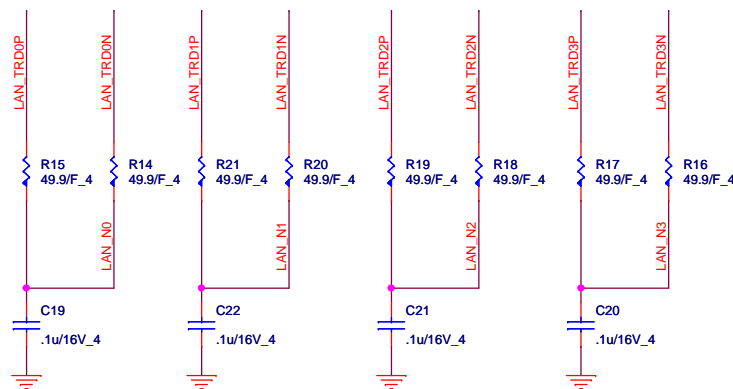
LAN Controller



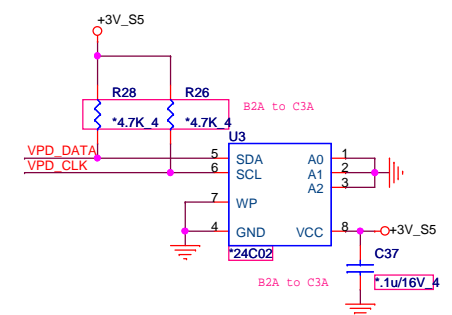
Decoupling CAP



PLACE NEAR IC SIDE

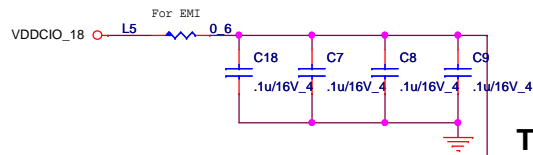


EEPROM

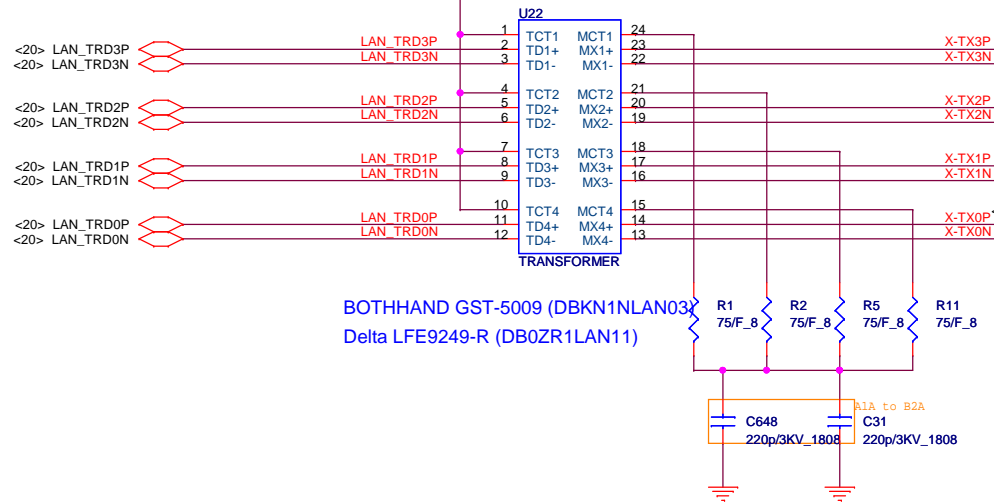


Quanta Computer Inc.
PROJECT : ZK6

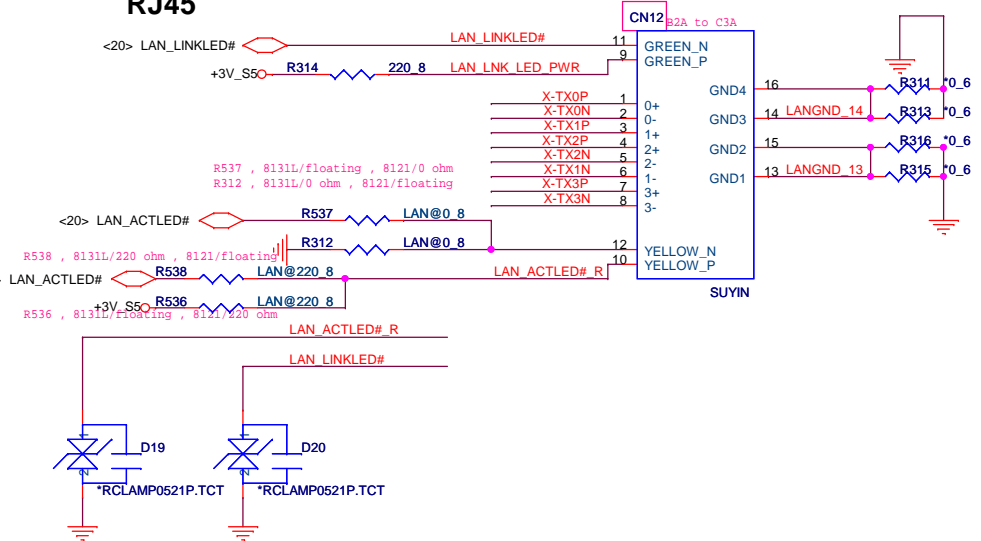
Size	Document Number	Rev
	AR8131 GLAN	1A
Date:	Friday, April 24, 2009	Sheet 20 of 42



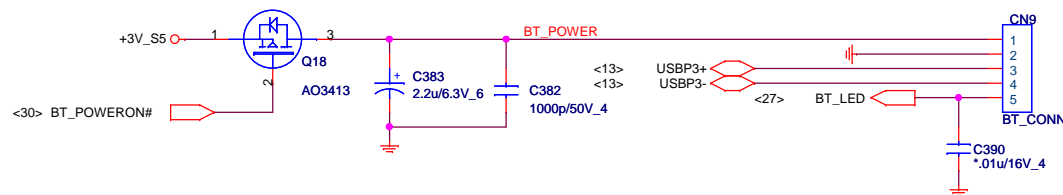
TRANSFORMER



RJ45



BLUETOOTH CONNECTOR



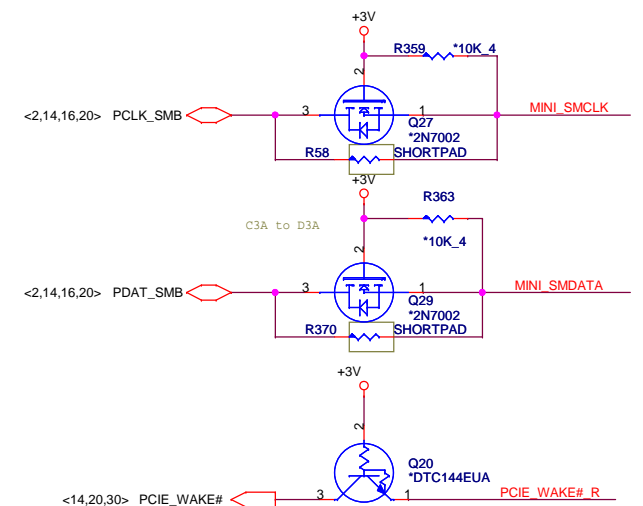
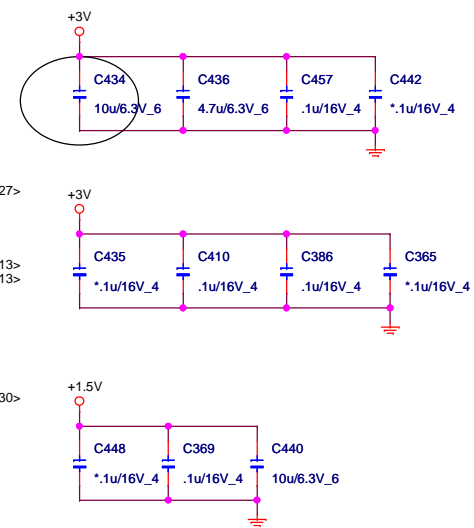
Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A

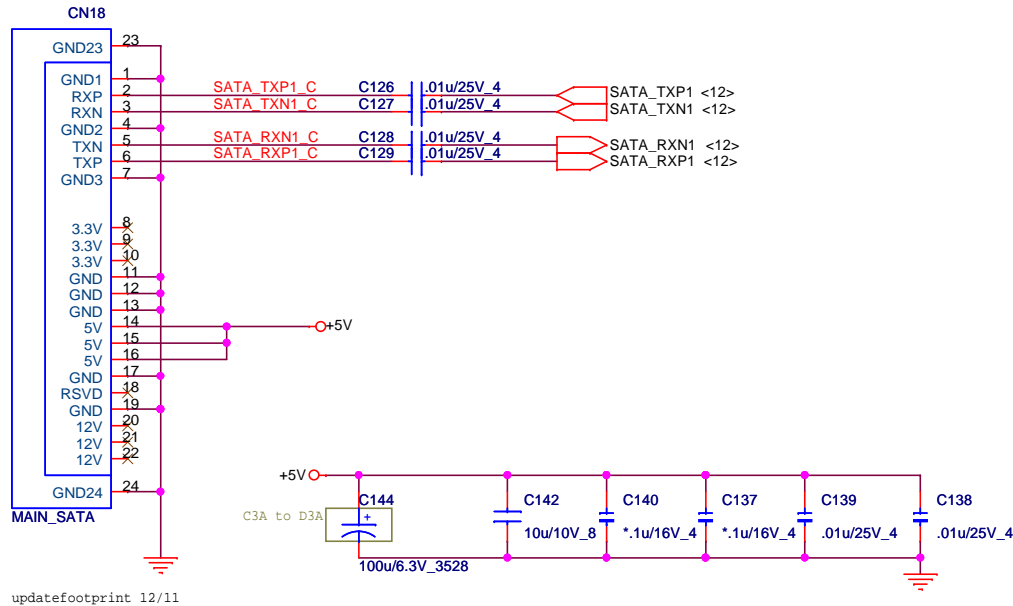
Date: Friday, April 24, 2009 Sheet 21 of 42

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

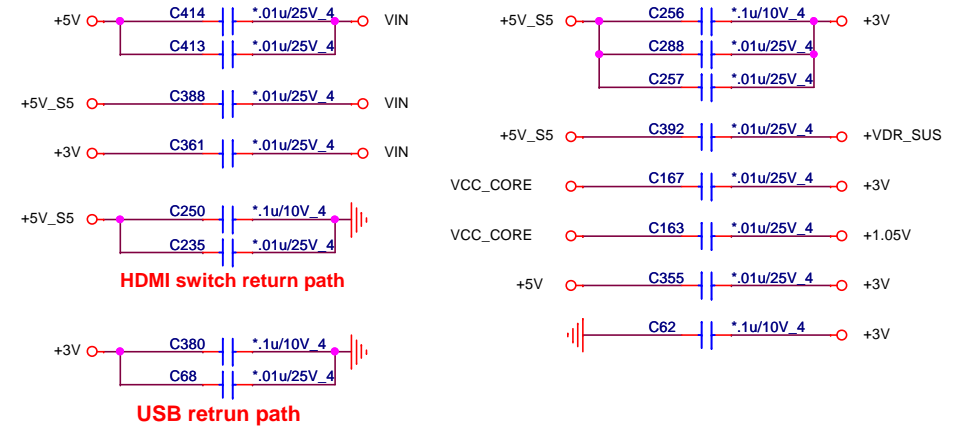


Size	Document Number	Rev
	MINI PCI-E card/TV	1A
Date:	Friday, April 24, 2009	Sheet 22 of 42

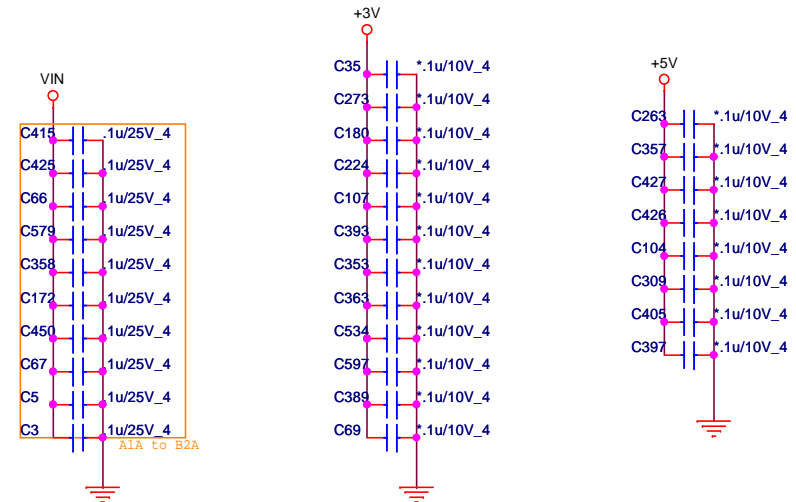
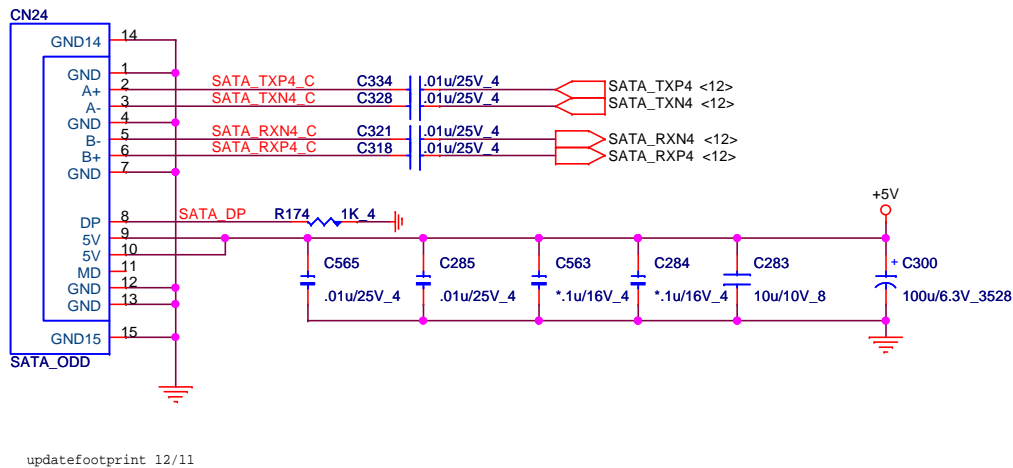
MAIN SATA HDD

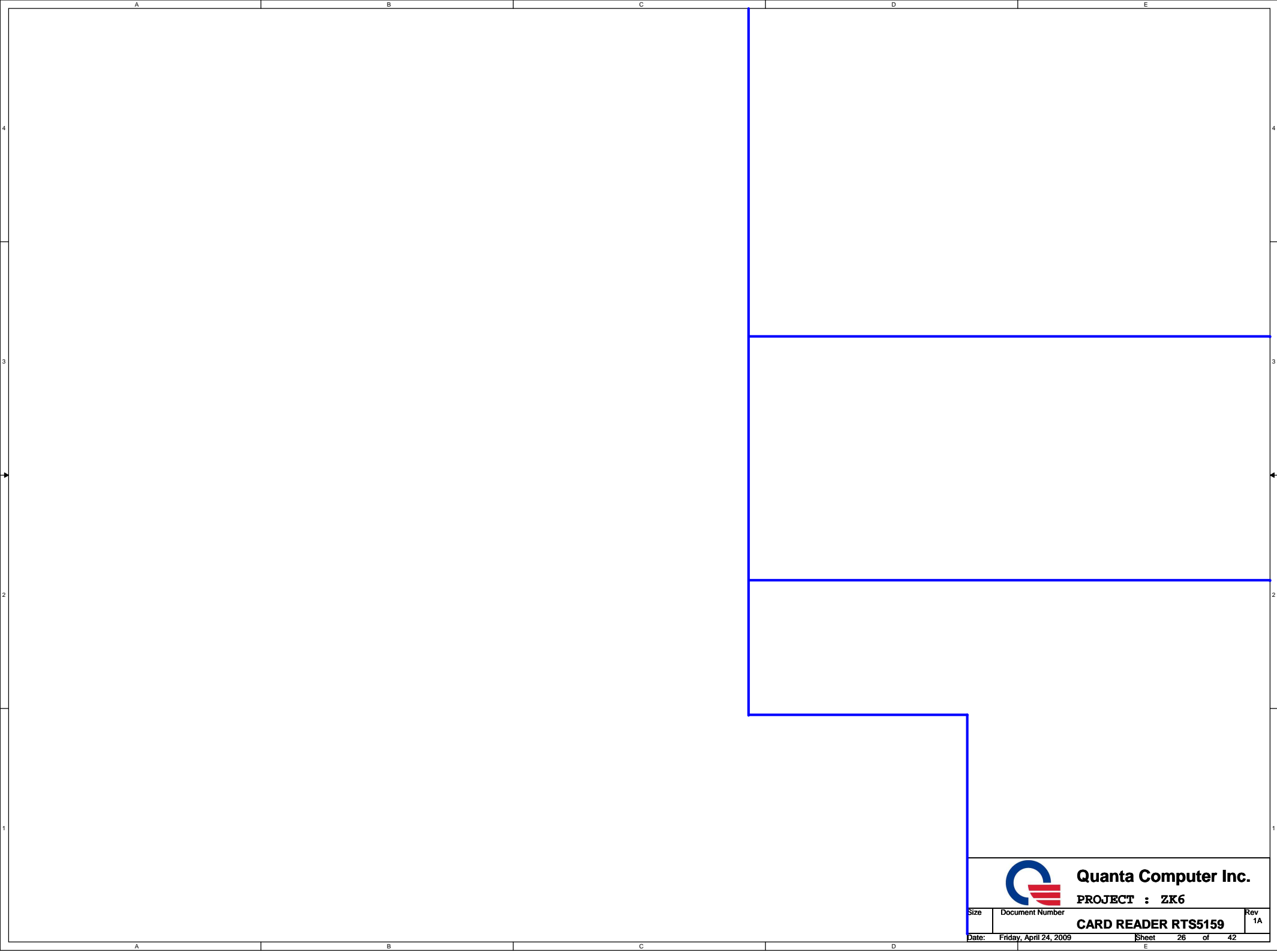


EE RETURN-PATH CAPACITORS

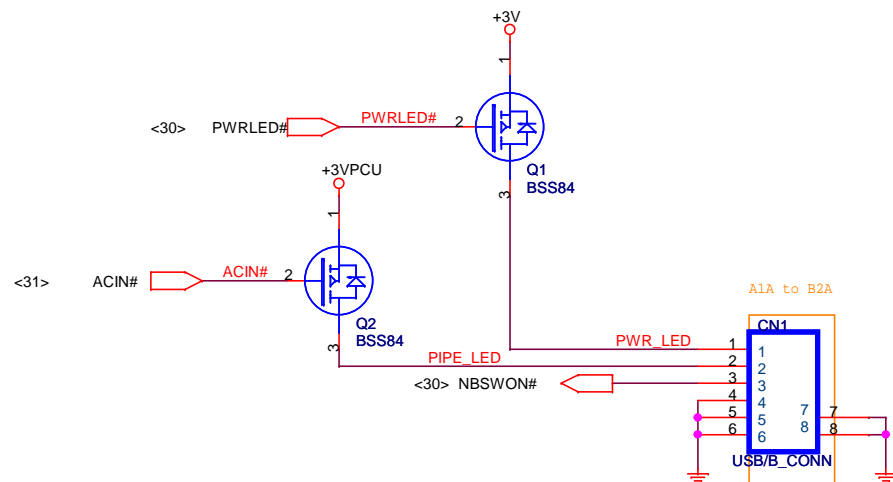


ODD (SATA)

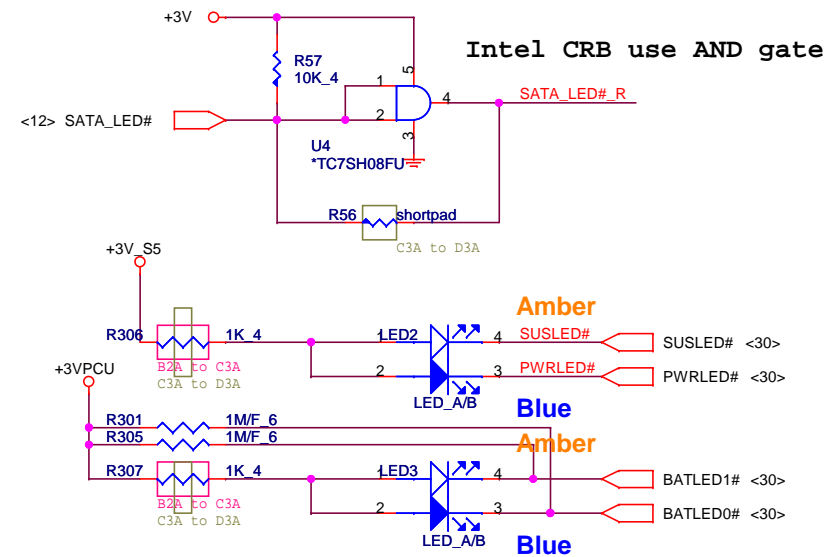




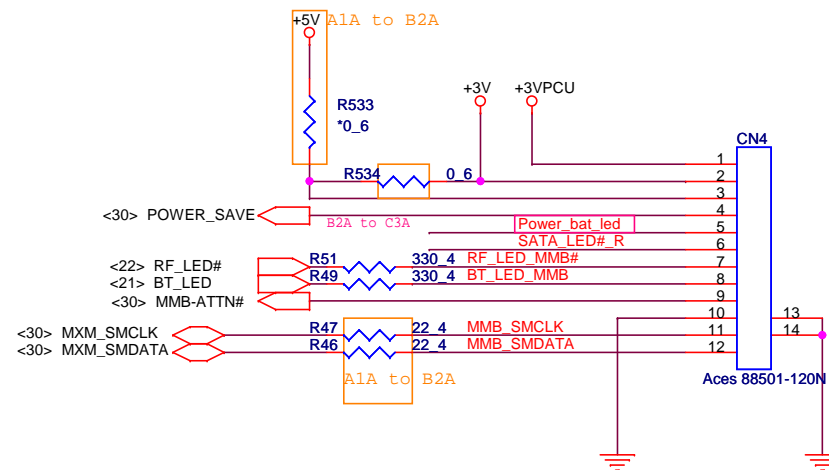
POWER BOARD



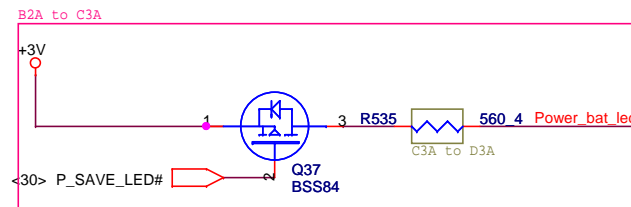
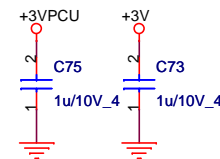
LED



MMB



Close to MMB connector

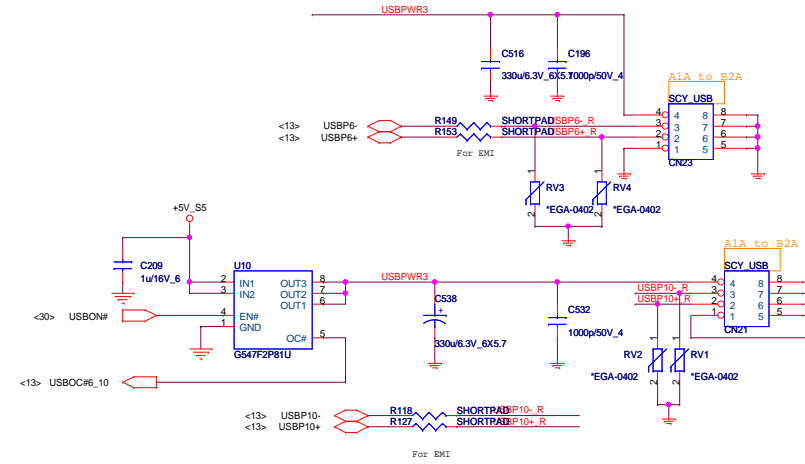


Quanta Computer Inc.

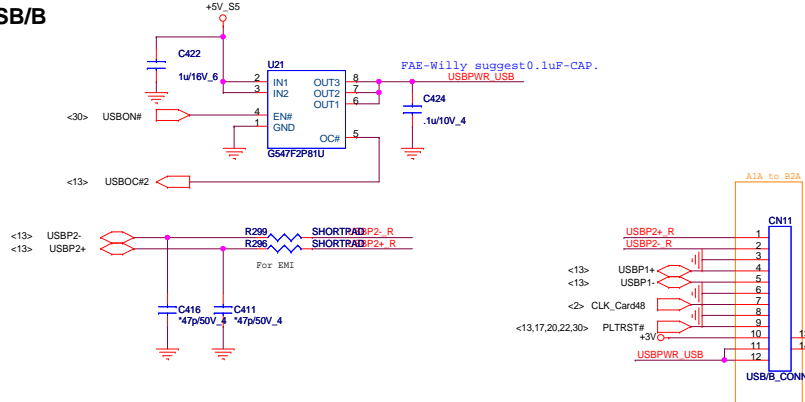
PROJECT : ZK6

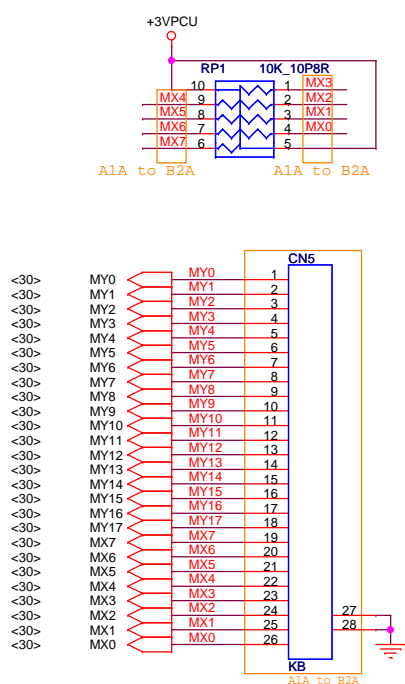
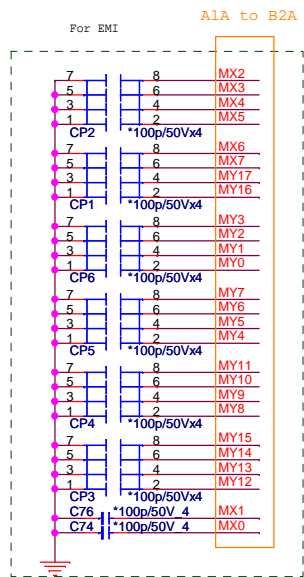
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date:	Friday, April 24, 2009	Sheet 27 of 42

USB PORT

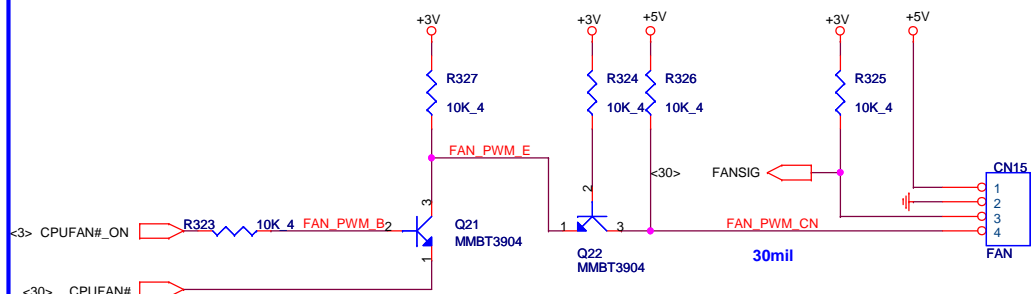


USB/B

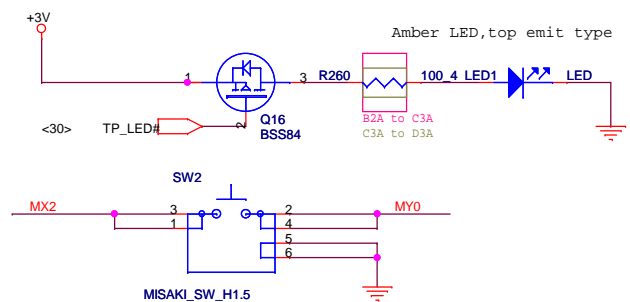




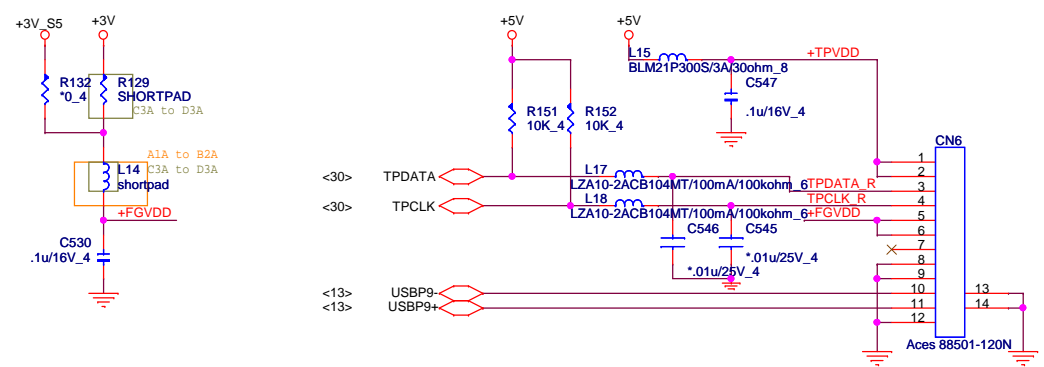
CPU FAN

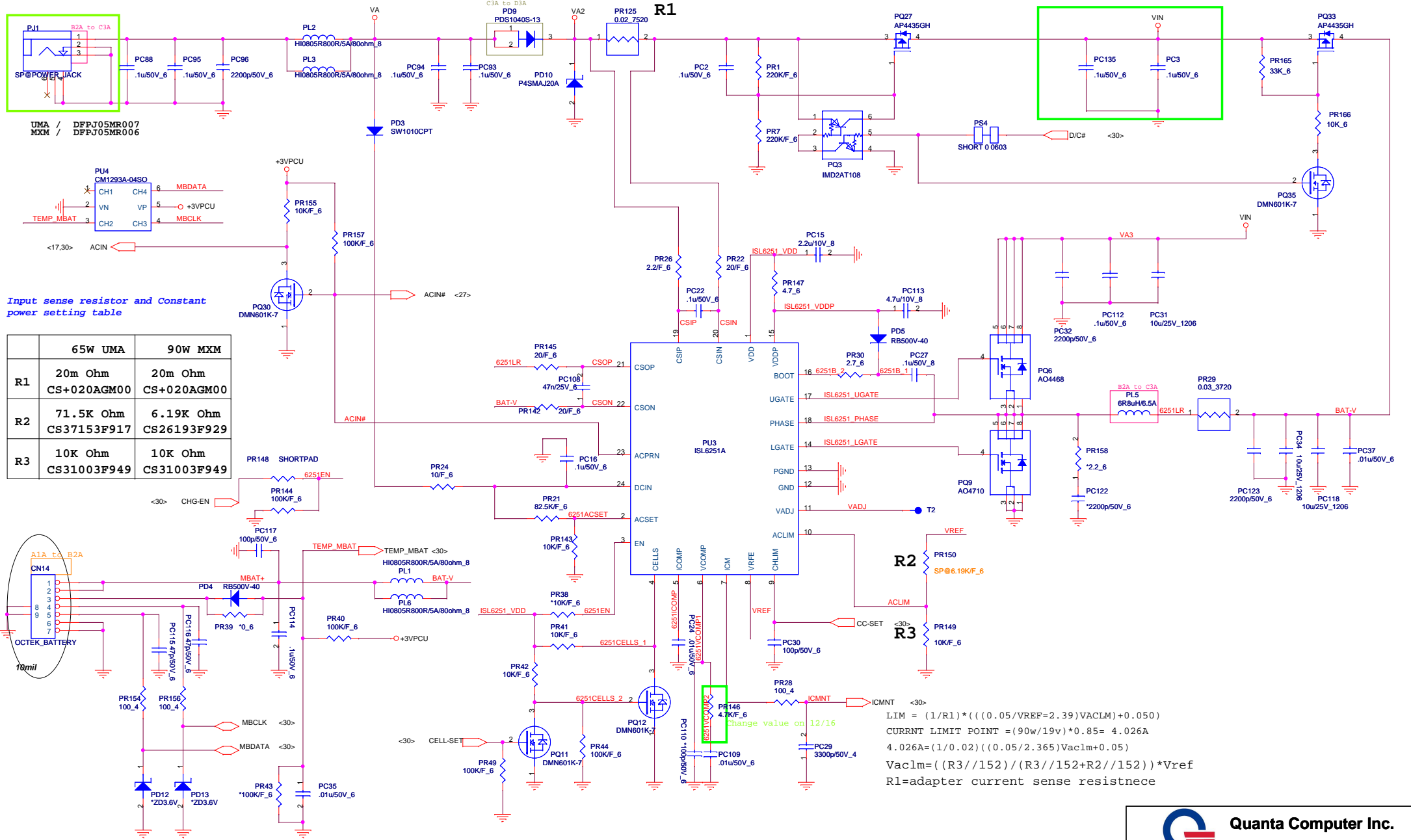


TP LOCK Button

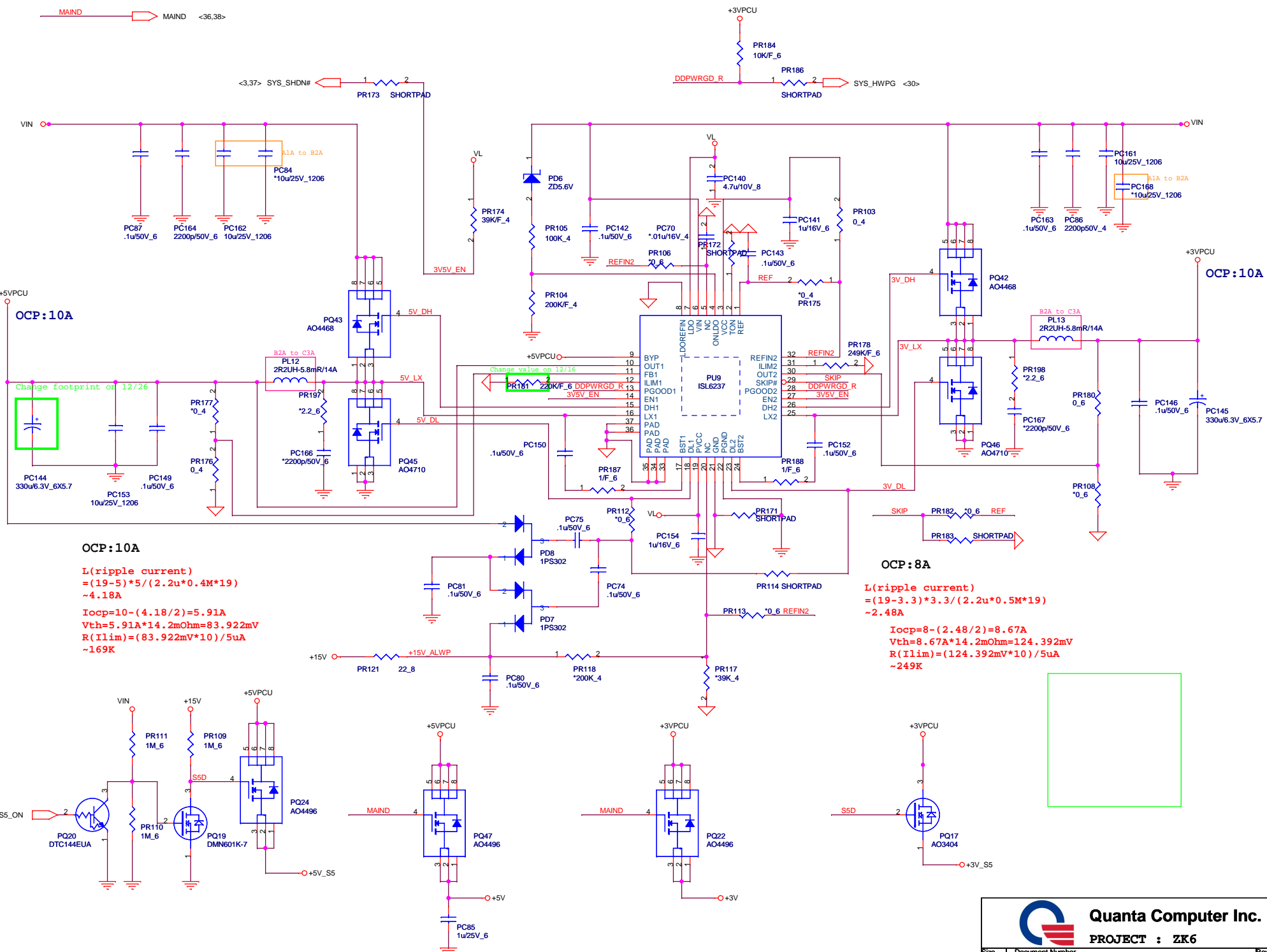


TOUCHPAD & Finger-Printer CONN.





CELL-SET = Hi ----- Cells = VDD ----->4S
CELL-SET = Low ----- Cells = GND ----->3S



OCP:10A

$L(\text{ripple current}) = (19-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 19) \sim 4.18 \text{A}$
 $I_{\text{ocp}} = 10 - (4.18 / 2) = 5.91 \text{A}$
 $V_{\text{th}} = 5.91 \text{A} \cdot 14.2 \text{m}\Omega = 83.922 \text{mV}$
 $R(\text{Ilim}) = (83.922 \text{mV} \cdot 10) / 5 \mu \text{A} \sim 169 \text{K}$

OCP:8A

$L(\text{ripple current}) = (19-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 19) \sim 2.48 \text{A}$
 $I_{\text{ocp}} = 8 - (2.48 / 2) = 8.67 \text{A}$
 $V_{\text{th}} = 8.67 \text{A} \cdot 14.2 \text{m}\Omega = 124.392 \text{mV}$
 $R(\text{Ilim}) = (124.392 \text{mV} \cdot 10) / 5 \mu \text{A} \sim 249 \text{K}$

all component in this page would be stuff for UMA only

